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INK JET PRINT HEAD IDENTIFICATION CIRCUIT AND METHOD

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 92105458, filed March 13, 2003.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention generally relates to an ink jet print head, and more particularly, to an identification circuit for the ink jet print head and a method thereof.

Description of Related Art

[0002] Different types of computer peripheral products have been developed and are now widely accepted. For ink jet printers, in order to fulfill different printing requirements for users working in different environments, different types of ink jet printers have been developed. However, each ink jet printer has different types of the ink jet print heads that correspond to it, for example, an ink jet print head with a black cartridge or color cartridge, and ink jet print heads with different number of injection nozzles.

[0003] In order to identify the types of the ink jet print head, an identification code corresponding to its model or serial number is given to each ink jet print head when it is manufactured, so that the ink jet printer can identify different types of ink jet print heads when they are installed onto the ink jet printer, so as to use different control programs to control the ink jet print heads of different models or serial numbers.

[0004] As described above, since there are many types of the ink jet print heads, an identification circuit that reads one or identification codes corresponding to its model or serial number had better be designed into the ink jet print head to provide the ink jet printer to identify different types of the ink jet print heads installed thereon. Since the identification circuit of the ink jet print head is only used at the moment of the ink jet print head being installed in the ink jet printer or before the first printing operation is started, and once the ink jet print head is identified, the identification circuit can be no longer used. Therefore, it is common that the identification circuit of the ink jet print head reads the identification code stored in the ink jet print head by using the address lines of the print head array.

[0005] FIG. 1 schematically shows a block diagram of an ink jet printer identification system. As shown in the drawing, the ink jet printer identification system 100 comprises printer electronics 110 and print head electronics 120, wherein the printer electronics 110 and the print head electronics 120 are connected with each other via a plurality of address lines 131 and a temperature sensing output line 132. The printer electronics 110 comprise a controller 111 and a driving circuit 112, and the print head electronics 120 comprise a print head array 121, an identification circuit 122, and a temperature sensing circuit 123.

[0006] When it is printing, the controller 111 transmits the data being printed to the driving circuit 112, and the driving circuit 112 drives the address lines 131, so as to control the print head array 121 to print out the required patterns. The temperature sensing circuit 123 senses the temperature of the print head, and transmits it to the controller 111 via the temperature sensing output line 132. The identification circuit 122 connected to part of the address lines 131 and is used to have the controller 111 send out a

control signal for reading out the stored identification code, and to output the stored identification code via the temperature sensing output line 132.

[0007] There are several types of the identification circuits in the prior art, the one shown in FIG. 2 is one identification circuit disclosed by U.S. Patent No. 5,363,134. As shown in the drawing, the identification circuit 200 comprises a plurality of programmable fuses F1 ~ F13 and a plurality of transistors Q1 ~ Q13. One end of each of the fuses F1 ~ F13 is coupled to a corresponding gate of the transistors Q1 ~ Q13, so as to control the "ON" or "OFF" of the transistors Q1 ~ Q13. The identification code corresponding to the type of the ink jet print head using this identification circuit 200 is stored via the programmable fuses F1 ~ F13. Whether each of the fuses F1 ~ F13 is fused or not represents a bit data of the identification code, respectively.

[0008] When the printer intends to read the identification code, a high level reading control signal is sent out via the address lines 131. Here, it is assumed that the high level reading control signal is sent out from A13. If the fuse F13 is reserved, the transistor Q13 is ON, therefore, the temperature sensing output line 132 is dropped down to a low level for reading an identification code of "0". On the contrary, if the fuse F13 is fused when it is programmed, the transistor Q13 is OFF, and the temperature sensing output line 132 is pulled up to a high level by the pull-up resistor (not shown) of the printer electronics 110 in FIG. 1. Therefore, an identification code of "1" is read out, and the method mentioned above can be used to sequentially read out other bits of the identification code.

[0009] Each address line of such type of the identification circuit 200 can only read out one corresponding bit of the identification code. Therefore, the quantity of the bits in the identification code that can be stored in the print head is limited by the number of the address lines, so it is hard to expand.

[0010] FIG. 3 shows the other identification circuit disclosed by U.S. Patent No. 5,940,095. The identification circuit 300 mainly comprises a plurality of one-bit shift registers 320a, 320b, 320c, and 320d for achieving the object of implementing a parallel in, serial out identification circuit. That is, when the printer electronics 110 in FIG. 1 transmits a loading control signal "Load" via the address line 325, the stored identification code is loaded in parallel to the plurality of one-bit shift registers 320a, 320b, 320c, and 320d. Then, when a first clock signal clk1 and a second clock signal clk2 are sequentially received via the address line 326 and 327, respectively, the bit data stored in the one-bit shift register 320d is shifted out via the output line 328. Then, the bit data stored in the one-bit shift register 320c is shifted into the one-bit shift register 320d, the bit data stored in the one-bit shift register 320b is shifted into the one-bit shift register 320c, and the bit data stored in the one-bit shift register 320a is shifted into the one-bit shift register 320b.

[0011] Therefore, after the printer electronics 110 transmits the loading control signal "Load", and sequentially transmits the required first clock signal clk1 and the required second clock signal clk2 via the address line 326 and 327, respectively, the identification code stored in the plurality of one-bit shift registers 320a, 320b, 320c, and 320d is output sequentially. Therefore, such parallel in, serial out identification circuit 300 is able to expand the bit number of the identification code based on the requirements with only small number of the address lines, such as 325, 326, and 327, so that it is not limited by the number of the address lines.

[0012] However, the identification circuit that is able to expand the bit number of the identification code and not be limited by the number of the address lines, is not limited in

implementation to the parallel in, serial out identification circuit by using the shift register mentioned above.

SUMMARY OF THE INVENTION

[0013] To solve the problem mentioned above, the present invention provides an identification circuit for identifying the ink jet print head and a method thereof. The bit number of the identification code can be expanded based on the requirements, and it is not limited by the number of the address lines.

[0014] In order to achieve the object mentioned above and others, the present invention provides an identification circuit for identifying the ink jet print head, wherein the identification circuit is suitable for use in an ink jet printer that comprises a reset signal line, at least one clock signal line, and an identification code signal line, so as to identify the type of the installed ink jet print head. The identification circuit comprises a counter, a logic unit, and a programming unit.

[0015] The counter is coupled to the reset signal line and at least one clock signal line. The counter is reset when the reset signal is received by the reset signal line, and the count value is counted to the next value when a corresponding clock signal is received by at least one clock signal line, so as to output it from a plurality of output terminals of the counter.

[0016] The logic unit comprises a plurality of input terminals and an output terminal. The output terminal is coupled to an identification code signal line, so as to output the identification code that represents the type of the ink jet print head. The programming unit is coupled to the output terminals of the counter and the input terminals of the logic

unit. The programming unit is used for programming a corresponding connection between each output terminal of the counter and the input terminals of the logic unit.

[0017] In an embodiment, after the counter is reset, the counter is counted in a sequence of 1, 2, 4, 8, 16, ..., to count its count value.

[0018] In an embodiment, the logic unit may be an OR gate, and the OR gate may comprise an enabling control terminal for accepting the control of the clock signal of the clock signal line.

[0019] In an embodiment, the programming unit is programmed in a mask programmed way when the identification circuit of the ink jet print head is being manufactured, so as to store the required identification code.

[0020] In another embodiment, the programming unit uses fuses to provide the programmable programming unit, so as to store the required identification code.

[0021] The present invention further provides an identification circuit for identifying the ink jet print head, wherein the identification circuit is suitable for use in an ink jet printer that comprises a reset signal line, at least one clock signal line, and an identification code signal line, so as to identify the type of the installed ink jet print head. The identification circuit comprises a counter, a plurality of switches, and a programming unit.

[0022] The counter is coupled to the reset signal line and at least one clock signal line. The counter is reset when the reset signal is received by the reset signal line, and the count value is counted to next value when a corresponding clock signal is received by the at least one clock signal line, so as to output it from a plurality of output terminals of the counter.

[0023] Each of the plurality of switches comprises an input terminal, an output terminal, and a control terminal. The output terminals of all switches are coupled to the

identification code signal line, so as to output the identification code that represents the type of the ink jet print head. The control terminal of each switch is coupled to the corresponding output terminal of the counter, so as to accept the control from the output terminal of the counter.

[0024] The programming unit coupled to the input terminal of the switch mentioned above is used for programming the input value that is input to the input terminal of the switch according to the identification code to be stored.

[0025] In an embodiment, after the counter is reset, the counter is counted in a sequence of 1, 2, 4, 8, 16, ..., to count its count value.

[0026] In an embodiment, the switch is made of a NMOS transistor or a CMOS transistor.

[0027] In an embodiment, the programming unit is programmed in a mask programmed way when the identification circuit of the ink jet print head is being manufactured, so as to store the required identification code.

[0028] In another embodiment, the programming unit uses fuses to provide the programmable programming unit, so as to store the required identification code.

[0029] Based on the spirit of the present invention, the present invention provides an identification method of the ink jet print head. The method is suitable for identifying the ink jet print head and comprises the steps of: providing a reset signal, and at least one clock signal; resetting a count value when the reset signal is received; counting a count value of the counter to next value when the at least one clock signal is received, and programming a logic circuit according to an identification code that represents the type of the ink jet print head and the count value mentioned above, so as to sequentially output the required identification code of the ink jet print head.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention. In the drawings,

[0031] FIG. 1 schematically shows a block diagram of an ink jet printer identification system.

[0032] FIG. 2 schematically shows a diagram of an identification circuit disclosed by U.S. Patent No. 5,363,134.

[0033] FIG. 3 schematically shows a diagram of another identification circuit disclosed by U.S. Patent No. 5,940,095.

[0034] FIG. 4 schematically shows a diagram of an ink jet print head identification circuit of the first embodiment according to the present invention.

[0035] FIG. 5 schematically shows an operation timing diagram of an ink jet print head identification circuit of the first and second embodiments according to the present invention.

[0036] FIG. 6 schematically shows a diagram of an ink jet print head identification circuit of the second embodiment according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] FIG. 4 schematically shows a diagram of an ink jet print head identification circuit of the first embodiment according to the present invention. As shown in the drawing, the identification circuit 400 comprises a counter 410; an OR logic unit 430 that

is, for example, constituted by an OR gate; and a programming unit 420 that is, for example, constituted by a plurality of fuses. Although fuses are used as the programming unit 420 in the drawing, it will be apparent to one of the ordinary skill in the art that the programming unit 420 also can be programmed in a mask programmed way when the identification circuit 400 of the ink jet print head is being manufactured, optionally, other methods also can be applied, such as laser trimming or fusing. It should be noted that electrical connectors or conductors can be used in the programming unit 420 instead of using fuses.

[0038] As shown in FIG. 4, the identification circuit 400 of the ink jet print head only use three address lines of the ink jet printer (not shown): the reset signal line 401 for transmitting the reset signal "Reset", the first clock signal line 402 for transmitting the first clock signal Clk1, and the second clock signal line 403 for transmitting the second clock signal Clk2, to perform the function of identifying the type of the installed ink jet print head. Therefore, the bit number of the identification code can be expanded based on its requirement, and is not limited by the number of the address lines.

[0039] The counter 410 is coupled to the reset signal line 401, the first clock signal line 402, and the second clock signal line 403. In the present embodiment, since the bit number required for the identification code is 8 bits, an 8-bit counter having 8 output terminals b0 ~ b7 is used for the required bit number of the identification code. Each of the output terminals b0 ~ b7 is coupled to one input terminal of the OR logic unit 430 via a fuse of the programming unit 420, respectively. Each of the input terminals of the OR logic unit 430 is grounded via a fuse of the programming unit 420, respectively, so that the required identification code can be stored by the programming. Further, the OR gate that constitutes the OR logic unit 430 can further comprise an enabling control terminal

EN to accept the control of the second clock signal Clk2 from the second clock signal line 403.

[0040] If it is assumed that the identification code to be stored is 11101000, the fuse F10, F11, F12, F3, F14, F5, F6, and F7 in the drawing should be fused, and the fuse F0, F1, F2, F13, F4, F15, F16 and F17 in the drawing should be reserved, so that the programming unit 420 can be programmed to store the required identification code. Its operation principle is described hereinafter referring to the operation timing diagram in FIG. 5.

[0041] When the counter 410 receives the reset signal "Reset" from the reset signal line 401, the count value of the counter 410 is reset to 0. When the counter 410 sequentially receives a first clock signal Clk1 and a second clock signal Clk2 from the first clock signal line 402 and the second clock signal line 403, respectively, the counter 410 counts its count value in a certain sequence, such as 1, 2, 4, 8, 16, ..., etc. That is, after the count value of the counter 410 is reset to 0, the output terminals b0 ~ b7 of the counter 410 are sequentially set as a high level "1" when a first clock signal Clk1 and a second clock signal Clk2 are sequentially received from the first clock signal line 402 and the second clock signal line 403, its operation timing is like b0 ~ b7 shown in FIG. 5.

[0042] When the output terminal b0 of the counter 410 is set to "1", and the output terminals b1 ~ b7 are "0", since the fuse F0 is reserved when it is programmed, the output terminal of the OR logic unit 430 outputs the identification code ID of "1". When the output terminal b1 of the counter 410 is "1", and the output terminals b0 and b2 ~ b7 are "0", since the fuse F1 is reserved when it is programmed, the output terminal of the OR logic unit 430 outputs the identification code ID of "1". Similarly, when the output terminal b2 of the counter 410 is "1", and the output terminals b0 ~ b1 and b3 ~ b7 are "0", since the fuse F2 is reserved when it is programmed, the output terminal of the OR logic

unit 430 outputs the identification code ID of "1". When the output terminal b3 of the counter 410 is "1", and the output terminals b0 ~ b2 and b4 ~ b7 are "0", since the fuse F3 is fused and F13 is reserved when they are programmed, the output terminal of the OR logic unit 430 outputs the identification code ID of "0". In the same way, the output terminal of the OR logic unit 430 sequentially outputs the identification code ID of "11101000", which represents the identification code of the installed ink jet print head, and its operation timing is as the ID shown in FIG. 5.

[0043] FIG. 6 schematically shows a diagram of an ink jet print head identification circuit of the second embodiment according to the present invention. As shown in the drawing, the identification circuit 600 comprises a counter 610; a programming unit 620 that is, for example, constituted by a plurality of fuses; and a plurality of switches 630, 631, 632, 633, 634, 635, 636, and 637 that are, for example, constituted by a plurality of the NMOS transistors. Although fuses are used as the programming unit 620 in the drawing, it will be apparent to one of the ordinary skill in the art that the programming unit 620 also can be programmed in a mask programmed way when the identification circuit 600 of the ink jet print head is being manufactured, optionally, other methods also can be applied, such as laser trimming or fusing. It should be noted that electrical connectors or conductors can be used in the programming unit 420 instead of using fuses.

[0044] As shown in FIG. 6, similarly the identification circuit 600 of the ink jet print head only use three address lines of the ink jet printer (not shown): the reset signal line 601 for transmitting the reset signal "Reset", the first clock signal line 602 for transmitting the first clock signal Clk1, and the second clock signal line 603 for transmitting the second clock signal Clk2, to perform the function of identifying the type of the installed ink jet print head. Therefore, the bit number of the identification code can

be expanded based on its requirement, and is not limited by the number of the address lines.

[0045] The counter 610 is coupled to the reset signal line 601, the first clock signal line 602, and the second clock signal line 603. In the present embodiment, since the bit number required for the identification code is 8 bits, an 8-bit counter having 8 output terminals b0 ~ b7 is used for the required bit number of the identification code. Each of the output terminals b0 ~ b7 is coupled to one gate of the corresponding switches 630, 631, 632, 633, 634, 635, 636, and 637, respectively, so as to control the "ON" or "OFF" of the switches 630, 631, 632, 633, 634, 635, 636, and 637, respectively. A source/drain of each of the switches 630, 631, 632, 633, 634, 635, 636, and 637 is respectively coupled to the power terminal or grounded via the fuse of the programming unit 620, so that the required identification code can be input by the programming. Further, the other source/drain of each of the switches 630, 631, 632, 633, 634, 635, 636, and 637 are coupled together to the identification code signal line 605, so as to output the identification code.

[0046] If it is assumed that the identification code to be stored is 11101000, the fuse F10, F11, F12, F3, F14, F5, F6, and F7 in the drawing should be fused, and the fuse F0, F1, F2, F13, F4, F15, F16 and F17 in the drawing should be reserved, so that the programming unit 620 can be programmed to store the required identification code. Its operation principle is described hereinafter referring to the operation timing diagram in FIG. 5.

[0047] When the counter 610 receives the reset signal "Reset" from the reset signal line 601, the count value of the counter 610 is reset to 0. When the counter 610 sequentially receives a first clock signal Clk1 and a second clock signal Clk2 from the first clock signal line 602 and the second clock signal line 603, respectively, the counter 610 counts

its count value in a certain sequence, such as 1, 2, 4, 8, 16, ..., etc. That is, after the count value of the counter 610 is reset to 0, the output terminals b0 ~ b7 of the counter 610 are sequentially set as a high level "1" when a first clock signal Clk1 and a second clock signal Clk2 are sequentially received from the first clock signal line 602 and the second clock signal line 603, respectively, its operation timing is like b0 ~ b7 shown in FIG. 5.

[0048] When the output terminal b0 of the counter 610 is set to "1", the switch 630 is ON, and since the fuse F0 is reserved when it is programmed, the identification code ID of "1" is output. When the output terminal b1 of the counter 610 is set to "1", the switch 631 is ON, and since the fuse F1 is reserved when it is programmed, the identification code ID of "1" is output. Similarly, when the output terminal b2 of the counter 610 is set to "1", the switch 632 is ON, and since the fuse F2 is reserved when it is programmed, the identification code ID of "1" is output. When the output terminal b3 of the counter 610 is set to "1", the switch 633 is ON, and since the fuse F3 is fused and fuse F13 is reserved when they are programmed, the identification code ID of "0" is output. In the same way, the identification code signal line 605 sequentially outputs the identification code ID of "11101000", which represents the identification code of the installed ink jet print head, and its operation timing is as the ID shown in FIG. 5.

[0049] It will be apparent to one of the ordinary skill in the art that the embodiments mentioned above are only some of the embodiments embodied the present invention. For example, the reference number 430 in FIG. 4 can be easily replaced with other logic unit (e.g. NAND logic unit) or decoder. Thus, it is not limited to use the OR logic unit. Similarly, the clock signal lines used in the present invention are not necessarily limited to using two signal lines. Optionally, it is possible to achieve the object and function of the present invention with only one clock signal line. Further, the switches 631 ~ 637 in

FIG. 6 are not limited to be implemented by the NMOS transistors. Optionally, it is also possible to implement the switches by using the CMOS transistors.

[0050] Based on the spirit of the embodiments mentioned above, an identification method of the ink jet print head is concluded. The method is suitable for identifying the ink jet print head and comprises the steps of: providing a reset signal, and at least one clock signal; resetting a count value when the reset signal is received; counting a count value of the counter to next value when the at least one clock signal is received, and programming a logic circuit according to an identification code that represents the type of the ink jet print head and the count value mentioned above, so as to sequentially output the required identification code of the ink jet print head.

[0051] Wherein, after the count value is reset to 0, and the first clock signal and the second clock signal are sequentially received, the count value is counted in a certain sequence, such as 1, 2, 4, 8, 16, ..., etc. Further, the logic circuit may be a logic gate or a plurality of NMOS or CMOS transistors.

[0052] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.